Advanced CMOS Process Technology

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Contents

Preface

The microelectronics revolution persists. Technical innovations abound, and the performance-to-cost ratios for semiconductor devices, integrated circuits, and systems continue to grow. Although it might be entertaining, a historical account of the past three decades of microelectronics would provide little direct benefit to the industry. This volume of the *VLSI Electronics* series, titled *Advanced CMOS Process Technology,* provides a current snapshot of one highly pertinent domain of microelectronics. For reasons discussed within the text, CMOS (complementary metal–oxide–semiconductor) technology plays a leading role in present and future electronic systems.

In choosing appropriate material for this monograph, we specified two selection criteria. First, we sought topics of primary importance to the present and future state of the art of CMOS process technology. Second, where constraints of space and time imposed on the number of topics to cover, we focused on issues with the least amount of coverage in other forums. Aside from introductory comments and background on CMOS device and circuit considerations, we narrowed our topic list to metallization, isolation techniques, reliability, and yield. The reader should not infer that omitted areas, including lithography and etching techniques, are of inferior rank. Rather, such topics have enjoyed a good deal of explicit scrutiny in, for example, earlier volumes of this *VLSI Electronics* series.

Finally, we note that it has been and is our goal to contribute to the global microelectronics industry by reporting as clearly as possible the present status of the CMOS process technology issues we chose to communicate. Furthermore, we attempted to project as accurately as possible expected future evolution. This contribution is transitory. We expect the industry to surpass the technical content of this monograph through innovation, invention, and, à la Thomas Edison, perspiration. In fact, we dedicate this volume to the engineers, scientists, and technical managers who will render obsolete many of the technical concerns we voice.

We express our deep gratitude to the General Electric Corporate Research and Development Center for many forms of support. Beyond merely countenancing our preparation of this manuscript as a tolerable extracurricular exercise, we felt a strongly supportive and encouraging environment. In particular, we thank William R. Cady and Kirby G. Vosburgh. The excellent and gracious secretarial skills of Elizabeth A. Harris and Marcia E. Vinick provided great assistance. One of us (JMP) acknowledges the continual encouragement of Harold J. Raveché (formerly Dean of Science at the Rensselaer Polytechnic Institute and now President of the Stevens Institute of Technology) and conversations with Igor Bol of the Xerox Corporation.

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Chapter 1

Introduction

We contemplate the microelectronics revolution of the twentieth century from a broad perspective. Current theories of evolution argue that the human race evolved from other animal species in a quantized manner. That is, evolution does not proceed at a uniform rate. Relatively short bursts of mutation punctuate longer periods of evolutionary dormancy. Such an understanding is consistent with the importance of fluctuations, deviations from the mean behavior, in nature. On a larger scale, distribution of matter in the universe is exceedingly nonuniform.

Advances in technology and human society also arrive in discrete steps. Consider the improvement of the standard of living in the past 200 years. The Industrial Revolution of the late nineteenth century yielded drastic productivity gains. With new inventions and manufacturing capability for farm equipment, agricultural production exploded as the need for human resources declined. Though many contemporary politicians would likely decry such a situation, society benefitted enormously. With the sudden drop in the human and economic price of agricultural production, both resources became available for the pursuit of "higher order" human needs such as medicine, manual labor reduction, and scientific research. The Industrial Revolution enabled this century's exponential population growth by loosening the shackle of one basic need.

It is also fair to say that the Industrial Revolution was a necessary precursor for all of the world's more recent technological gains. These gains include advances in medical techniques, transportation, electronics, microelectronics (one portion of which is the focus of this monograph), and biotechnology. Would any wise person have predicted most of these benefits in the initial stages of the Industrial Revolution? We think not. The point of this question is that advances in technology will likely precipitate

many gains in society beyond those that are easily recognized. We must therefore list anticipated benefits of any technology, as we will later for CMOS microelectronics, with humility.

Electronics, and particularly microelectronics, spawned the field of numerical computation. It is difficult to imagine the lack of such capability as recently as 40 years ago. Richard Feynman and R. Leighton recounted the method of computation of this era [1]. To evaluate a mathematical expression expressing a result of theoretical physics required a roomful of technicians and an assembly line operation. Such tasks today require inexpensive calculators. Computers in the worlds of finance, accounting, marketing, retailing, etc., greatly expedite previously expensive tasks. Beyond this tremendous increase in productivity arose the new methodology of numerical computation for solving previously intractable scientific, engineering, and mathematical problems.

Attempts to enumerate a representative, let alone complete, list of benefits of microelectronics to the development of technology and society are futile. Telecommunications has enjoyed revolutionary expansion. Numerical solution of mathematical models relevant to fluid flow, semiconductor physics, and optimization have drastically reduced the design costs of airplanes and automobiles, semiconductor devices, and sundry manufacturing processes. Many consumer products, including automobiles, now contain microprocessors for improved reliability and performance. Noninvasive medical imaging techniques, such as the computer-assisted tomography (CAT) scan, magnetic resonance, and ultrasound imaging, require sophisticated computational capability. Productivity in the office environment and publishing industries has surged forward with the advent of computer-assisted typing and text processing. On a "slow" day, the New York Stock Exchange trades two hundred million shares of stock with current automated trading systems. Ironically, some interested observers blame computers for the near collapse of the financial system on October 19–20, 1987. Such an assessment is inaccurate because the computer system merely executed the instructions of several of the largest pension funds and brokerage houses.

As the reader suspects by now, the two key benefits of technological advances are increased productivity (for established tasks) and spontaneous creation of new capabilities. Improvement in the standard of living of the human race can arise only from increased productivity [2]. Government decree, legislation, or regulation that does not benefit productivity cannot improve the economic well-being of citizens. Furthermore, watershed events such as the Industrial Revolution and microelectronics revolution, which precipitate gigantic leaps in the standard of living, can only germinate, blossom, and grow in the fertile ground of political, personal,

and economic freedom. The justification of this statement lies in the nature of technological breakthroughs. Such breakthroughs begin as accidental experimental findings, ingenious ideas, straightforward adaptation of existing technologies, or some combination of these elements. It is never clear in these early stages if any useful product or process will eventually emerge. In fact, it is most likely that nothing useful will emerge. For every great invention we celebrate exist thousands that failed to match its inventor's hopes.

Frankly, there is no person or group of people smart enough to reliably predict which emerging ideas will succeed (i.e., benefit society) and which will not. Only society can decide by its reaction to the new product in the free market. Who brings the product to market? Assuming the existence of political and personal freedom, the inventor is entitled to do so. (In the absence of such freedom, the oppressive government may appropriate the idea in the unlikely circumstance that the inventor chooses to make this disclosure.) To bring his/her product to market, the inventor must invest the necessary capital. Thus, the inventor assumes financial risk and stands to gain or lose in concert with the technical or market success of the product. Where innovation is required, this system functions well since the inventor has great motivation (i.e., his/her own financial well-being) to invent and bring to market a product in a form that best meets society's needs. Furthermore, the inventor is disinclined to pour capital into an idea that, as is most likely, is failing because of technical or market reasons. Government intervention, even in a predominantly free market, dampens this process and depresses the standard of living. An apparently innocuous government program of lessening the risk to the inventor (by subsidy, for example) is still detrimental since the inventor is likely to waste more money before abandoning his/her project. The inventor understandably considers the taxpayer's money as disposable.

The relationship between political, personal, and economic freedom and microelectronics motivates our brief foray into economic issues. As much or more so than other technological areas, microelectronics requires a great deal of innovation. The technical challenges have been, are, and will be formidable. Continued progress feeds on brilliant ideas of scientists and engineers of many disciplines and flexibility and calculated risk-taking of corporate managers. Freedom is essential to progress in microelectronics. A quick survey of world microelectronics finds the dominant activity in North America (United States and Canada), Southeast Asia (Japan and South Korea), and western Europe. With the possible exceptions of Hong Kong and Taiwan, this list corresponds to that of the regions of greatest economic freedom. Western Europe lags North America and Southeast Asia primarily because of restrictions on economic freedom of its citizens.

Similarly, the technical backwardness of socialist countries in eastern Europe, Asia, and the Third World does not stem from any inherent deficiency of the citizens of these countries. Rather, the absence of economic freedom intrinsic to socialism and the loss of political freedom, which generally accompanies socialism, do not permit the necessary innovation. Of course, the problems of the Third World go far beyond a failure to foster microelectronics growth. The standard justification for barriers to free trade in the Third World is the need to "protect" the fragile economy. It is this protection and other socialist measures that have impoverished a large fraction of the human race. The continuing tragedy of starvation in Ethiopia is abetted by the counter-productive, dogmatic policies of the socialist government.

Having explored the social context of technological advances in general and microelectronics in particular, we will focus now, and for the remainder of this monograph, on technical aspects. Microelectronics is the discipline of designing and fabricating electrical circuits from discrete components integrated into a single semiconductor sample. This field owes its existence to many scientific and engineering accomplishments. Two of these are the inventions of the metal–oxide–semiconductor field-effect transistor (MOSFET) in the 1930s and the bipolar transistor in the 1940s. Electrical circuits previously constructed with discrete components wired together or with vacuum tubes as circuit elements are much less expensive, and hence more readily employed, with the advent of microelectronics. Furthermore, microelectronics allows the construction of previously impractical or impossible circuits.

Requirements of a particular application generally dictate the choice between MOS and bipolar technologies. The main advantages of bipolar circuits are fast switching and high current drive, while MOS enjoys higher input impedance, lower power dissipation, and greater packing density. The MOS technology has gradually displaced bipolar technology in many applications but will not do so completely. There will always exist situations, such as central processor units, in which high speed is critical. We will focus on the most promising aspect of MOS technology. Though beyond the scope of this manuscript, we alert the reader to recent attempts to merge MOS and bipolar technologies within the same substrate [3].

The three categories of metal–oxide–semiconductor (MOS) technology are NMOS (*n* channel), PMOS (*p* channel), and CMOS. Our choice of MOS technology implies a restriction to silicon as the semiconductor material because of its ability to form uniform oxide layers of high quality. The semiconductor substrate of *n*-channel devices is *p*-type, while that of *p*-channel devices is *n*-type. Electrons are the dominant charge carrier for current flow in *n*-channel devices, while holes pay a similar role in *p*-chan-

nel technology. Complementary metal–oxide–semiconductor (CMOS) technology employs both *n*-channel and *p*-channel devices, while NMOS (PMOS) is exclusively *n* channel (*p* channel).

PMOS served as the primary technology for the first MOS circuits in the late 1960s. Since the silicon–silicon dioxide interface tends to develop a positive charge [4], the PMOS choice allows effortless fabrication of enhancement-mode (negative threshold voltage) devices, and this property ingratiated PMOS with the semiconductor world. Improved methods of impurity diffusion and ion implantation soon allowed the fabrication of NMOS enhancement-mode devices. NMOS quickly displaced PMOS in view of the inherently higher mobility of electrons relative to holes [5]. The higher mobility allows greater performance (i.e., current drive, switching speed) for equal circuit size or smaller circuit size for equal performance with NMOS as opposed to PMOS. Inherent advantages of PMOS include relative insensitivity to ionizing radiation and reduced hot carrier instability. This latter observation coupled with the reduced disparity between electron and hole mobilities in the high electric fields of short-channel MOSFETs even prompted the suggestion that PMOS may be the superior technology as MOSFET channel lengths decrease [6]. This prediction will likely never be realized since PMOS possesses other disadvantages in terms of short-channel device fabrication. It is difficult to fabricate shallow source–drain junctions with conventional *p*-type dopants in silicon. For other material reasons, it is also more challenging to fabricate $p+$ polysilicon gates for PMOS than it is to fabricate $n+$ polysilicon gates for NMOS.

The debate between NMOS and PMOS superiority in the short-channel limit is not of great importance since there exist overwhelming advantages for CMOS technology. In fact, all submicron MOS technology will be CMOS so that one might have easily entitled this book "Advanced MOS Process Technology." CMOS circuit design combines *n*-channel and *p*-channel devices in such a manner to reduce the standby current by orders of magnitude relative to pure NMOS or PMOS implementations. We discuss this justification of CMOS at length in Chapter 2. Suffice it to say for now that the heat removal problem associated with power dissipation in NMOS and PMOS circuits poses a formidable barrier. Other advantages of CMOS include system complexity, circuit considerations, and device reliability issues. The greatest CMOS disadvantages arise from the design and processing layout for closely spaced *n*-channel and *p*-channel devices with the ever present constraint of latch-up immunity. Again, Chapter 2 will focus on these issues.

The microelectronics industry has struggled, and continues to struggle, to reduce the physical dimensions of individual devices. In CMOS fabrication, such a goal implies the realization of short-channel MOS field-effect

transistors (*n* channel and *p* channel) as well as adequate, high-density methods for interconnecting these devices. Diminution of circuits and whole systems results from the scale reduction of individual devices. Economic forces drive this miniaturization. Size reduction permits fabrication of a greater number of chips per wafer with generally a higher percentage yield of defect-free products. For reasons directly and indirectly tied to device size, circuit and system performances improve as devices shrink. Competition requires manufacturers to strive continually to upgrade their product through miniaturization and pass the manufacturing cost savings onto the consumer. The introduction and dramatic technical and economic metamorphosis of the hand-held calculator in the 1970s serves as an excellent example of the evolution of semiconductor manufacturing. The personal computer of the 1980s distributed and decentralized an enormous amount of computational power. Engineering work stations employ the latest technology to pack the memory and power of a superminicomputer into a desktop unit. Industry executives and analysts now (early 1988) discuss plans for desktop supercomputers.

Successful definition and development of a CMOS fabrication process with reduced design rules require the integration of many individual efforts. One must develop the basic tools of metallization, isolation techniques, lithography, etching, and impurity profile adjustment. Device size reduction exacerbates several device reliability mechanisms and hence necessitates device and circuit design to assure reliability. Finally, one must identify applications and design circuits to capitalize on the miniaturized fabrication process. This last task is not, as one might suspect, trivial. Certainly there do exist some functions, such as memory, for which the motives and design methods of miniaturization are evident. Identification of new and previously impractical circuit *and* system concepts rendered feasible by advances in process technology is essential. Such identification requires great ingenuity and can provide the raison d'être for investment in advanced process development.

Convenient forums for definition of past, present, and future technology are two ubiquitous circuits known as the dynamic random access memory (DRAM) and static random access memory (SRAM). Both the DRAM and SRAM are two-dimensional arrays of memory cells. The SRAM cell consists of two inverters with additional FETs for array addressing. The DRAM cell requires only a FET and capacitor per cell and hence is more compact. Memory retention in the DRAM is, however, unstable (i.e., dynamic), so that the peripheral circuitry and system must bear the burden of periodically refreshing the stored information. Both SRAMs and DRAMs find wide application in computational systems. Since the SRAM

and DRAM cell designs have changed very little in the past 15 years, advances in process technology propagate quickly to these memory chips. Device reduction allows more memory per area of silicon.

Armed with a 12-μm design rule manufacturing process, Intel marketed a SRAM with 256 bits (cells) of memory in 1969. Toshiba announced a 256-K SRAM in 1984 with a 1.2-μm process [7]. The SRAM performance as measured by cell access time improved by a factor of 20, while the storage capacity ballooned by three orders of magnitude. Figure 1.1 portrays this trend graphically [8]. From similarly humble beginnings, 1-M (one megabit) DRAMs have emerged and are now available on the open market. Quite symbolic is the restriction of the "old" and still pervasive personal computer operating system MS-DOS to 640 kbytes of dynamic memory. The hardware outstripped the software to the point that this operating system cannot handle one bank of dynamic memory chips. SRAMs with 1-M capacity and DRAMs at 4 M will require a 0.8-μm design rule process with some increase in chip size. Recent reports discuss technology development [7] and reduction to practice in the laboratory [9] for this high-density DRAM. With innovative solutions for, or elegant sidestepping of, alpha particle immunity, reliability concerns, and subthreshold leakage problems, continued device reduction will produce DRAMs in the 16–64-M range.

We have documented the benefit of reduced feature size in CMOS

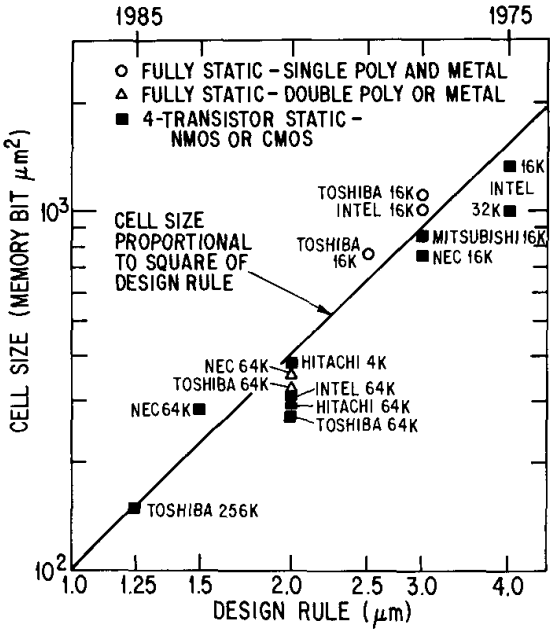

Fig. 1.1. We depict continued SRAM miniaturization as originally presented by Brown *et al.* [8]. © 1986 IEEE.

microelectronics. Given the enormous investment required to investigate and develop high-resolution fabrication processes, contemplation and prediction of ultimate limits become invaluable guides in planning technical goals. Fundamental and practical limits will conspire to frustrate miniaturization at some as yet unspecified level. Examples of fundamental limits are the thermal voltage fluctuations of the order of kT/q and the turn-on slope of a forward-biased diode. Practical limits are far more vexing and include identifying metals with a highly restrictive set of properties and the formation of ultrashallow source–drain junctions. We direct the reader to review Banerjee and Bordelon [10] for an excellent and philosophical discussion of this subject.

Furthermore, the ultimate minimum device size will certainly be a function of the specific design philosophy and application [11–13]. Consideration of noise immunity permits shorter channel lengths in digital logic circuits implemented in enhancement/enhancement CMOS, for example, as compared to enhancement/depletion CMOS [11]. Logic gates in turn are relatively insensitive to subthreshold leakage. This leakage contributes mainly to undesirable power dissipation in this implementation. In transmission gates, however, and particularly in dynamic memory cells, subthreshold conduction can destroy the desired function. Present theoretical estimates find that silicon MOSFETs with effective channel lengths in the area of 0.1 μm and exceedingly low subthreshold conduction at room temperature are manufacturable given the appropriate and presently unavailable technology [14]. A recent research effort has successfully produced a 0.1-μm channel length MOSFET for low-temperature operation [15].

In this monograph, we seek to describe the present state of the art in the technical areas most relevant and unique to advanced CMOS process technology. We give a brief background discussion on device and circuit considerations in Chapter 2. Our hope is that the reader will find this section useful for subsequent appeals to fundamental knowledge in later chapters. Chapter 3 discusses choices and techniques for metallization based on numerous practical constraints and considerations. Interconnection of short-channel devices is, of course, crucial to full realization of density gains in miniaturization. Dimensional reduction of metal lines is fraught with difficulties related to etching, reliability, and performance issues. We also focus on the improved technique of unframed contacts for density enhancement. Chapter 4 reviews the most important and promising isolation techniques. Such techniques are of central importance to present and future CMOS technology since the requirement of latch-up immunity opposes the goal of high packing density. We devote an extended discussion to reliability concerns (hot carriers, electromigration,

and oxide wear-out) in Chapter 5. One must recognize reliability as an essential ingredient of technological development in the earliest phase. An exposition of yield in present and future advanced CMOS processes in Chapter 6 concludes this volume.

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Chapter 2

CMOS Device and Circuit Background

Fabrication of the MOSFET is arguably the central theme of the CMOS process flow. Virtually all manufacturing steps seek to define the MOSFET structure, isolate adjacent MOSFETs, and interconnect and passivate MOSFETs. The preponderance of this basic device in CMOS digital and analog circuits necessitates this processing focus.

When we speak of CMOS miniaturization and design rule reduction, the first and foremost consideration is the fabrication of smaller MOSFETs with improved isolation and interconnection techniques. Physical delineation of ever smaller structures by advances in lithography, etching, ion implantation, and metallization is certainly a major challenge. These issues spring easily to mind in any reflection on advanced CMOS processing techniques.

But there is much more to the subject of processing techniques. Mere fabrication of small structures ignores the driving motivation of producing the next generation of low-cost, superior performance integrated circuits. Device performance considerations must assume great importance during conception and definition of the CMOS process flow. In addition, low cost requires assurance of device and circuit reliability and high manufacturing yield. Thus, one must view superior performance, reliability, and high yield as specifications of the process flow on an equal footing with more conventional requirements, such as nominal MOSFET gate length and minimum lithographic feature size.

Subsequent chapters will address the physical delineation issues of metallization and device isolation as well as reliability and yield. This chapter will first discuss device physics relevant to the formulation of an advanced CMOS fabrication process. Our goal is to provide a complete discourse on

this specialized topic to which the reader may refer while studying other chapters of this text. We also recommend the more expansive books by Sze [1], Grove [2], Ghandhi [3], and Nicollian and Brews [4]. We then address CMOS circuit design considerations and compare the CMOS and NMOS technologies. A description of the CMOS latch-up mechanism follows.

While it is reasonable to consider the MOSFET as the most fundamental device in any CMOS process, one's physical understanding is facilitated by considering the junction diode and the MOS capacitor. The next two sections discuss these basic devices. We follow with a description of the MOSFET. Beyond the description of MOSFET operation, we analyze the concepts of scaling theory and the related issue of short-channel effects.

I. JUNCTION DIODE

The great utility of semiconducting materials stems from the ease with which one may alter material conduction properties. Substitution of impurities such as phosphorus, arsenic, and antimony from column V of the periodic table for the host atoms of an elemental (column IV) semiconductor, even in small concentrations, drastically enhances the density of electrons in the semiconductor conduction band. This impurity "doping" renders the electron density far greater than the hole density since column V (donor) impurities essentially donate electrons to the host semiconductor. A hole is simply an unfilled electron energy state in the semiconductor valence band. Introducing impurities such as boron and gallium from column III of the periodic table has precisely the opposite effect. These column III (acceptor) impurities essentially remove electrons from the valence band and leave behind holes.

Consider the thought experiment in which we produce two semiconductor samples. In one sample, we introduce a uniform concentration of donor impurities, while, in the other, we specify a uniform concentration of acceptor impurities. In both specimens, the total charge density is zero. While the *n*-type (donor impurity) sample has many more electrons than holes, the total negative charge of this electron-to-hole excess is exactly compensated by the positively charged donor impurities. Similarly, the *p*-type (acceptor impurity) sample excess hole positive charge is exactly compensated by the negatively charged acceptor impurities.

Suppose we bring the *n*-type and *p*-type silicon samples into intimate contact. What happens? The conduction band electrons and valence band holes are free to move by drift or diffusion while the charged impurities are immobile. Electrons and holes will quickly begin diffusing into the *p* region and *n* region, respectively, because of the large concentration gradients.